Cheng-Yu (Mike) Tsai

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Education

Georgia Institute of Technology
Atlanta, Georgia, USA

Doctor of Philosophy in Electrical and Computer Engineering — *Aug. 2024 - current*

- Advisor: Dr. Sung-Kyu Lim
- Experience: Electronic Design Automation (EDA), specialized in standard cell development and parasitic extraction

National Taiwan University
Taipei, Taiwan

Master of Science in Computer Science and Information Engineering — *Feb. 2019 - Jun. 2021*

- Advisor: Dr. Chia-Lin Yang
- Thesis: A Performance Analytical Model for DNN Training with Focus on Memory Subsystem
- Key words: Deep Neural Network, training, bandwidth, cache capacity, analytical model, data reuse

National Taiwan University
Taipei, Taiwan

Double degree of B.S.E in Electrical Engineering & B.S. in Computer Science and Information Engineering — *Sep. 2014 - Jan. 2019*

- GPA: 3.96/4.3 (3.84/4.0)
- Rank: 49/190 (26%)
- Awarded Presidential Award (semester GPA within top 5%) twice

Research Interests

Primary Electronic Design Automation (EDA), Computer architecture, Soft/Hardware co-design

Secondary Distributed Computing, Emerging Memory

Working Experience

Taiwan Semiconductor Manufacturing Company (TSMC)
Hsinchu, Taiwan

Engineer, Custom Design Flow Development Department, Design Technology Platform (DTP), R&D — *Jul. 2021 - Jul. 2024*

- Built a **delay calculator**, which takes DSPF as input and calculates the timing within a standard cell. This in-house method is more than 10x faster for delay or 100x faster for setup time than conventional spice simulation without commercial licenses while maintaining more than 0.9 of the ranking correlation coefficient.
- Built a **fully automated flow** to verify silicon photonics process design kit (PDK). This project integrates pre-layout simulation, schematic-driven layout, LVS, DRC, and RC extraction into a one-button task. At least 20x efficiency gain is expected than manual maneuver.
- Developed PDK utilities in N2 and N3 nodes

National Taiwan University
Taipei, Taiwan

Part-time worker, Division of Network Management, Computer & Information Networking Center — *Apr. 2018 - Jan. 2021*

- Built and maintained **VisQWL**: a Visualization framework for monitoring the Quality of campus-wide WireLess service. The heat map can easily pinpoint the hot spot of Wi-Fi usage, guide the system administrators about resource arrangement, and provide a tool to deal with user complaints.
- Skills: SNMP, Kibana, Elasticsearch, data visualization, wireless network, map data processing
- The work is published in a regional conference TANet30, and is online serving at https://ccnet.ntu.edu.tw/wireless/ (Chinese only)

Teaching Experience

Computer Architecture
National Taiwan University

Three-credit mandatory course for third-year undergraduate students — *Fall '19 and Fall '20*

- Offering a Verilog training lecture to enable students to be capable of working on their projects
- Introducing Verilog projects, clarifying students' confusion throughout the process, and grading their projects upon submission
- Drafting midterm and final exams and grading them
- Offering office hours for students to ask questions
- Setting up presentation and video recording devices for the instructor

Research Projects

A Performance Analytical Model for DNN Training with Focus on Memory Subsystem

MS Thesis

Exploring the tradeoffs between cache capacity and memory bandwidth in DNN workloads *Feb '19 - Jun '21*

- The first work to model data reuse across DNN layers in DNN workloads for 100+ MB cache
- Devised a novel software-controlled cache analytical scheme to approximate an optimal hardware design so that the architecture problem can be decoupled from low-level design issues.
- Analyzed tradeoffs between cache capacity and bandwidth in ResNet, MobileNet, GNMT, and Transformer and drew some insights from the experiment results.

Standard Cell Delay Calculator

Internal Project at TSMC

A model to swiftly estimate the delay of a post-layout standard cell (MOS + parasitic R/C) *Jun '22 - Jul '23*

- More than 10x faster than SPICE transient simulation, 100x faster than bi-section setup time simulation, while maintaining more than 0.9 of correlation coefficient and sub-ps accuracy with SPICE.
- Integrated graph theory, transient pre-characterization, layout dependent effect (LDE) estimation, asymptotic waveform evaluation, calculation on RC network and simplification, etc., into a single program to estimate propagation delay from a detailed standard parasitic format (DSPF) file.
- Leveraged parallel programming, scientific computing, inter-process communication and binding between C++ and Python, and various techniques to assure optimal efficiency and ease of use.
- Independently inquiring into influential factors while striking a balance between the model's efficiency and accuracy.

Honors & Awards

2024	**DTP Best Patent Award**, TSMC	*Hsinchu, Taiwan*
2022	**DTP Outstanding Procedure Innovation Award**, TSMC	*Hsinchu, Taiwan*
2016	**Presidential Award**, National Taiwan University	*Taipei, Taiwan*
2015	**Presidential Award**, National Taiwan University	*Taipei, Taiwan*